Remarks

Reconsideration of this Application is respectfully requested.

Applicants respectfully request admission of the foregoing amendment to place the application in condition for allowance by traversing the rejections under 35 U.S.C. §§ 102 and 103.

Upon entry of the foregoing amendment, claims 1-6 are pending in the application, with claim 1 being the independent claims. Claims 1 and 6 are sought to be amended. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Rejections Under 35 U.S.C. § 102

The Office Action rejected claims 1, 2, and 4-6 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,977,798 to Zerbe (hereinafter "Zerbe"). (*See* Office Action at p. 2.) Applicants respectfully traverse these rejections.

Amended independent claim 1 recites (emphasis added):

> A latch circuit, comprising:
>
> a bistable pair of transistors with both transistors connected directly between a reset switch and ***a node***, and having ***a first port*** for receiving a first current signal and producing a first output voltage, and a second port for receiving a second current signal and producing a second output voltage; and
>
> a vertical latch including a first transistor and a second transistor, each of said first transistor and said second transistor having a control terminal, a first non-control terminal, and a second non-control terminal, said control terminal of said first transistor connected directly to said first non-control terminal of said second transistor ***at said first port***, said control terminal of

> said second transistor connected directly to said first non-control terminal of said first transistor, and said second non-control terminal of said first transistor connected directly ***to said node***, wherein said first transistor is a first type, said second transistor is a second type, and said first type is different from said second type.

Zerbe does not disclose, teach, or suggest a latch circuit having a bistable pair of transistors and a vertical latch in which the bistable pair of transistors has both transistors connected directly between a reset switch and a node and the vertical latch includes a first transistor and a second transistor, each of the first transistor and the second transistor having a control terminal, a first non-control terminal, and a second non-control terminal, the control terminal of the first transistor connected directly to the first non-control terminal of the second transistor at the first port, the control terminal of the second transistor connected directly to the first non-control terminal of the first transistor, and the second non-control terminal of the first transistor connected directly to the node, such that the first transistor is a first type, the second transistor is a second type, and the first type is different from the second type.

Therefore, Zerbe does not anticipate claim 1. Because each of claims 2 and 4-6 depends upon claim 1 and because of the additional distinctive features of each of claims 2 and 4-6, each of these claims is also not anticipated by Zerbe. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejections of claims 1, 2, and 4-6 under 35 U.S.C. § 102(b) and pass these claims to allowance.

Rejections Under 35 U.S.C. § 103

The Office Action rejected claim 3 under 35 U.S.C. § 103(a) as being unpatentable over Zerbe in view of U.S. Patent Application Publication No. 2001/0048141 to Lin *et al.* (hereinafter "Lin"). (*See* Office Action at p. 3.) Applicants respectfully traverse this rejection.

Claim 3 depends upon claim 1. As stated above, Zerbe does not disclose, teach, or suggest a latch circuit having a bistable pair of transistors and a vertical latch in which the bistable pair of transistors has both transistors connected directly between a reset switch and a node and the vertical latch includes a first transistor and a second transistor, each of the first transistor and the second transistor having a control terminal, a first non-control terminal, and a second non-control terminal, the control terminal of the first transistor connected directly to the first non-control terminal of the second transistor at the first port, the control terminal of the second transistor connected directly to the first non-control terminal of the first transistor, and the second non-control terminal of the first transistor connected directly to the node, such that the first transistor is a first type, the second transistor is a second type, and the first type is different from the second type. Lin does not overcome this deficiency.

Therefore, claim 1 is patentable over Zerbe in view of Lin. Because claim 3 depends upon claim 1 and because of the additional distinctive features of claim 3, this claim is also patentable over Zerbe in view of Lin. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection of claim 3 under 35 U.S.C. § 103(a) and pass this claim to allowance.

Conclusion

All of the stated grounds of rejection have been properly traversed. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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